What is claimed is:

1. A method of forming a TFT device, comprising the steps of:

providing a substrate;

performing a first patterning procedure with a first photomask to form a first semiconductor island and a second semiconductor island on part of the substrate;

performing a second patterning procedure with a second photomask to expose the first semiconductor island and/or the second semiconductor island;

doping impurities into the exposed first semiconductor island and/or the exposed second semiconductor island to adjust threshold voltage;

forming an insulating layer on the first semiconductor island, the second semiconductor island and the substrate;

forming a conductive layer on the insulating layer;

performing a third patterning procedure with a third photomask to remove part of the conductive layer and define a first gate and a second gate;

using the first gate and the second gate as a mask, performing an n^--ion doping procedure to form an LDD region in the first semiconductor island;

performing a fourth patterning procedure with a fourth photomask to expose the second gate;

using the second gate as a mask, performing a p^+-ion doping procedure to form a second source/drain region in the second semiconductor island;

forming a passivation layer on the insulating layer, the first gate, and the second gate;

performing a fifth patterning procedure with a fifth photomask to form a plurality of contact holes penetrating the passivation layer and the insulating layer; and

by means of the contact holes, performing an n^+-ion doping procedure to form a first source/drain region in the first semiconductor island;

wherein an ion dosage of the p^+-ion doping procedure is greater than an ion dosage of the n^+ ions doping procedure.

2. The method according to claim 1, further comprising the step of:

filling a conductive material in the contact holes to form a plurality of plugs;

wherein the plugs electrically connect the first source/drain region or the second source/drain region.

3. The method according to claim 1, further comprising, before forming the first and second semiconductor islands, the step of:

forming a buffer layer on the substrate.

4. The method according to claim 3, wherein the buffer layer includes a silicon nitride layer and a silicon oxide layer.

5. The method according to claim 1, wherein the first and second semiconductor islands include silicon.

6. The method according to claim 1, wherein the insulating layer includes a silicon nitride layer and a silicon oxide layer.

7. The method according to claim 1, wherein the conductive layer is a metal layer.

8. The method according to claim 1, wherein the ion dosage of the p^+-ion doping procedure is ten times greater than that of the n^+-ion doping procedure.

9. The method according to claim 1, wherein the passivation layer is a silicon nitride layer or a silicon oxide layer.

10. A method of forming a CMOS TFT device with five photomasks, comprising steps of:

providing a substrate;

performing a first patterning procedure with a first photomask to form a first semiconductor island and a second semiconductor island on part of the substrate;

performing a second patterning procedure with a second photomask to expose part of the first semiconductor island and/or the second semiconductor island;

doping impurities into the exposed first semiconductor island and/or the exposed second semiconductor island to adjust threshold voltage;

forming a gate insulating layer on the first semiconductor island, the second semiconductor island and the substrate;

forming a conductive layer on the gate insulating layer;

performing a third patterning procedure with a third photomask to remove part of the conductive layer and

define a first gate and a second gate, wherein the first gate is located above the first semiconductor island and the second gate is located above the second semiconductor island;

using the first gate and the second gate as a mask, performing an n^--ion doping procedure to form an LDD region in the first semiconductor island;

performing a fourth patterning procedure with a fourth photomask to expose the second gate;

using the second gate as a mask, performing a p^+-ion doping procedure to form a second source/drain region in the second semiconductor island;

forming a passivation layer on the insulating layer, the first gate, and the second gate;

performing a fifth patterning procedure with a fifth photomask, and forming a plurality of contact holes penetrating the passivation layer and the insulating layer, wherein the contact holes are located above the first semiconductor island and the second semiconductor island; and

by means of the contact holes, performing an n^+-ion doping procedure to form a first source/drain region in the first semiconductor island;

wherein an ion dosage of the p^+-ion doping procedure is ten times than that of the n^+-ion doping procedure.

11. The method according to claim 10, further comprising the step of:

filling a conductive material in the contact holes to form a first plug, a second plug, a third plug and a fourth plug;

wherein the first and second plugs electrically connect the first source/drain region and the third and fourth plugs electrically connect the second source/drain region.

12. The method according to claim 10, further comprising, before forming the first and second semiconductor islands, the step of:

forming a buffer layer on the substrate.

13. The method according to claim 12, wherein the buffer layer includes a silicon nitride layer and a silicon oxide layer.

14. The method according to claim 10, wherein the insulating layer includes a silicon nitride layer and a silicon oxide layer.

15. The method according to claim 10, wherein the conductive layer is a metal layer.

16. The method according to claim 10, wherein the passivation layer is a silicon nitride layer or a silicon oxide layer.